AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application;

--1. (Currently Amended) A semiconductor memory device of a dynamic type for refreshing information stored in a memory space, so as to hold the information continuously by amplifying the information stored in said memory space to rewrite the amplified information in said memory space, said memory device comprising:

a refresh control circuit for performing refreshment of the information only to a ~~sub-memory~~ submemory space, which is in use when the refreshment of the information is performed, said ~~sub-memory~~ submemory space holding the information necessary to be refreshed, selected from among a plurality of ~~sub-memory~~ submemory spaces formed by a previous division of said memory space.

--2. (Currently Amended) A semiconductor memory device of a dynamic type including a memory cell array for storing information, and a refresh circuit for refreshing the information stored in said memory cell array, so as to hold the information continuously, by amplifying the information stored in said memory cell array to rewrite the amplified information in said memory cell array, said memory device comprising:

a refresh control circuit for controlling an operation of

said refresh circuit so as to perform refreshment of the information only to a ~~sub memory~~ submemory space ~~which~~ that is in use when the refreshment of the information is performed, said ~~sub memory~~ submemory space holding the information necessary to be refreshed, among a plurality of ~~sub memory~~ submemory spaces formed by previous division of an address space in a memory space of said memory cell array.

--3. (Currently Amended) The semiconductor memory device according to claim 2, wherein said refresh control circuit ~~operates~~ performs a logical product of data pertaining to whether each of said ~~sub memory~~ submemory spaces are in use ~~or not~~ and refresh address data to be input to each address, and performs control of whether said refreshment is performed or not to each ~~sub memory~~ submemory space with said refresh circuit based on ~~a basis of~~ a result of said ~~operation~~ logical product.

--4. (Currently Amended) The semiconductor memory device according to claim 2, wherein ~~a row decoder is added to~~ said memory cell array includes a row decoder, and said row decoder is set to specify a row address to which said refreshment is performed in addresses of said memory cell array, and ~~further~~ wherein said refresh control circuit is inserted between said memory cell array and said row decoder, said refresh control

circuit being set to intervene in a function of said row decoder for specifying the row address to which said refreshment is performed so as to control whether said refreshment is performed ~~or not~~ to each of said ~~sub memory~~ submemory spaces.

--5. (Currently Amended) The semiconductor memory device according to claim 2, wherein ~~a row decoder is added to~~ said memory cell array includes a row decoder, and said row decoder is set to specify a row address to which said refreshment is performed in addresses of said memory cell array, and ~~further~~ wherein said refresh control circuit is provided in said row decoder, said refresh control circuit being set to intervene in a function of said row decoder for specifying the row address to which said refreshment is performed so as to control whether the refreshment is performed ~~or not~~ to each of said ~~sub memory~~ submemory spaces.

--6. (Currently Amended) The semiconductor memory device according to claim 2, wherein ~~a row decoder and a refresh address counter are added to~~ said memory cell array includes a row decoder and a refresh address counter, and said row decoder and said refresh address counter are set to specify a row address to which said refreshment is performed in addresses of said memory cell array, and ~~further~~ wherein said refresh

control circuit is attached to said refresh address counter, said refresh control circuit being set to intervene in a function of said refresh address counter for outputting the row address to which said refreshment is performed so as to control whether the refreshment is performed ~~or not~~ to each of said ~~sub memory~~ submemory spaces.

--7. (Currently Amended) The semiconductor memory device according to claim 2, wherein ~~a row decoder and a refresh address counter are added to~~ said memory cell array includes a row decoder and a refresh address counter, and said row decoder and said refresh address counter are set to specify a row address to which said refreshment is performed in addresses of said memory cell array, and ~~further~~ wherein said refresh control circuit is provided inside said refresh address counter, said refresh control circuit being set to intervene in a function of said refresh address counter for outputting the row address to which said refreshment is performed so as to control whether the refreshment is performed ~~or not~~ to each of said ~~sub memory~~ submemory spaces.

--8. (Currently Amended) The semiconductor memory device according to claim 2, ~~wherein~~ further comprising a row decoder, a multiplexer and a refresh address counter [[are]] connected in order to said memory cell array ~~in this order~~, and said row

decoder, said multiplexer and said refresh address counter are set to specify a row address to which said refreshment is performed in addresses of said memory cell array, and ~~further~~ wherein said refresh control circuit is inserted between said refresh address counter and said multiplexer, said refresh control circuit being set to intervene in a refresh address counter's output of the row address to which said refreshment is performed, the output being transmitted to said row decoder through said multiplexer, so as to control whether the refreshment is performed ~~or not~~ to each of said ~~sub memory~~ submemory spaces.

--9. (Currently Amended) The semiconductor memory device according to claim 2, ~~wherein~~ further comprising a row decoder, a multiplexer and a refresh address counter [[are]] connected in order to said memory cell array ~~in this order~~, and said row decoder, said multiplexer and said refresh address counter are set to specify a row address to which said refreshment is performed in addresses of said memory cell array, and ~~further~~ wherein said refresh control circuit is provided inside said multiplexer, said refresh control circuit being set to intervene in a refresh address counter's output of the row address to which said refreshment is performed, the output being transmitted to said row decoder through said multiplexer, so as to control whether the refreshment is performed ~~or not~~ to

each of said ~~sub-memory~~ submemory spaces.

--10. (Currently Amended) The semiconductor memory device according to claim 2, wherein said memory space is ~~previously~~ divided into ~~different~~ a plurality of memory spaces to store ~~different~~ respective kinds of contents of information different from one another, and at least one of said ~~divided~~ plurality of memory spaces [[are]] is further divided into said plurality of ~~sub-memory~~ submemory spaces.

--11. (Currently Amended) A refresh control circuit ~~to be used~~ for a semiconductor memory device of a dynamic type for refreshing information stored in a memory space, so as to hold the information continuously, by amplifying the information stored in said memory space to rewrite the amplified information in said memory space,

wherein said refresh control circuit performs control of refreshment of the information only to a ~~sub-memory~~ submemory space, which is in use when the refreshment of the information is performed, said ~~sub-memory~~ submemory space holding the information necessary to be refreshed, selected from among a plurality of ~~sub-memory~~ submemory spaces formed by ~~previous~~ a division of said memory space.

--12. (Currently Amended) A refresh control circuit ~~to be~~

~~used~~ for a semiconductor memory device of a dynamic type including a memory cell array for storing information and a refresh circuit for refreshing the information stored in said memory cell array, so as to hold the information continuously, by amplifying the information stored in said memory cell array to rewrite the amplified information in said memory cell array,

wherein said refresh control circuit controls an operation of said refresh circuit so as to perform refreshment of the information only to a sub memory space which is in use when the refreshment of the information is performed, said ~~sub memory~~ submemory space, holding the information necessary to be refreshed, said submemory space being selected from among a plurality of sub memory spaces formed by previous division of an address space in a memory space of said memory cell array.

--13. (Currently Amended) The refresh control circuit according to claim 12, wherein said refresh control circuit ~~operates~~ performs a logical product of data pertaining to whether each of said sub memory spaces are in use ~~or not~~ and refresh address data to be input to each address, and performs control of whether said refreshment is performed ~~or not~~ to each ~~sub memory~~ submemory space with said refresh circuit based on ~~a basis of~~ a result of said ~~operation~~ logical product.

--14. (Currently Amended) The refresh control circuit

according to claim 12, wherein said memory space is ~~previously~~ divided into ~~different~~ a plurality of memory spaces to store ~~different~~ respective kinds of contents of information different from one another, and at least one of said divided memory spaces [[are]] is further divided into said plurality of ~~sub memory~~ submemory spaces.

--15. (Currently Amended) A method for refreshing storage in a semiconductor memory device of a dynamic type for refreshing information stored in a memory space, so as to hold the information continuously, by amplifying the information stored in said memory space to rewrite the amplified information in said memory space, said method comprising the steps of:

dividing said memory space into a plurality of ~~sub-memory~~ submemory spaces ~~in advance~~; and

performing refreshment of the information only to a ~~sub memory~~ selected submemory space among the plurality of ~~sub memory~~ submemory spaces, said ~~sub-memory~~ selected submemory space being in use when the refreshment of the information is performed, said ~~sub-memory~~ submemory space holding the information necessary to be refreshed.

--16. (Currently Amended) A refresh method for refreshing information stored in a memory cell array, so as to hold the

information continuously, by amplifying the information to rewrite the amplified information in said memory cell, said memory cell array [[is]] being provided in a semiconductor memory device of a dynamic type, said method comprising the steps of:

dividing an address space in a memory space of said memory cell array into a plurality of ~~sub memory~~ submemory spaces ~~in advance~~; and

performing refreshment of the information only to a ~~sub memory~~ selected submemory space among the plurality of ~~sub memory~~ submemory spaces, said ~~sub memory~~ selected submemory space being in use when the refreshment of the information is performed, said ~~sub memory~~ submemory space holding the information necessary to be refreshed.

--17. (Currently Amended) The refresh method according to claim 16, ~~wherein~~ comprising the further step of performing a logical product of data pertaining to whether each of said sub memory spaces is in use ~~or not~~ and refresh address data to be input to each address ~~is operated~~, [[and]] wherein control of whether said refreshment is performed ~~or not~~ to each ~~sub memory~~ submemory space is performed based on ~~a basis of~~ a result of said ~~operation~~ logical product.

--18. (Currently Amended) The refresh method according to

claim 16, wherein said memory space is ~~previously~~ divided into ~~different~~ a plurality memory spaces to store ~~different~~ respective kinds of contents of information different from one another, and at least one of said divided memory spaces is further divided into the plurality of ~~sub memory~~ submemory spaces to perform control of said refreshment of the information to each of said ~~sub memory~~ submemory spaces.